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JP 030192801 A

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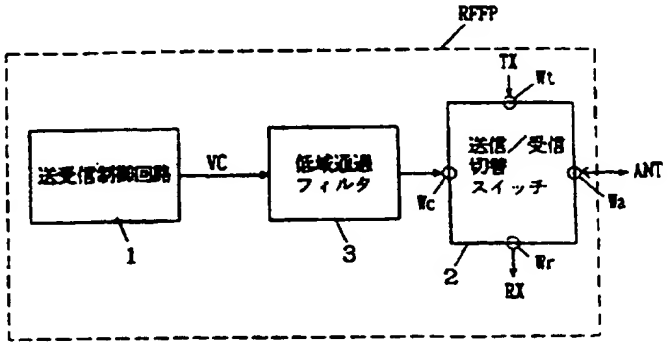
JITSUYO SHINAN KOHO 1926-1996
KOKAI JITSUYO SHINAN KOHO 1971-1996

(54) Abstract Title
High frequency intergrated circuit for high-frequency radio transmitter-receiver suppressed in influence of high-frequency power leakage

(57) A low-pass filter (3;3a, 3b; 8:13; 14) which only passes signals in a band lower than that of high-frequency signal components is provided between a high-frequency signal processing circuit (2; PAi) which processes the high-power signal of an RF front end section (RFFP) for processing the high-frequency signal of a portable telephone set and a control circuit (1: GVC) which controls the operation of the circuit (2). The circuit (2) functions as the transmission/reception switching circuit (2) of the telephone set and the circuit (1) functions as the transmission/reception control circuit (1) which determines the operation mode of the circuit (2). Alternatively, the circuit (2) functions as a power amplifier (PAi) and the control circuit (1) functions as the gate voltage control circuit (GVC) which adjusts the gain of the amplifier (PAi). Therefore, the influence of leakage of high-frequency components from the gate of a field effect transistor is suppressed, and the RF front end section (RRFP) can be constituted of a chip occupying a small area.



1 ... transmission-reception control circuit

2 ... transmission/reception switch

3 ... low-pass filter

GB 2 331 879 A

図1

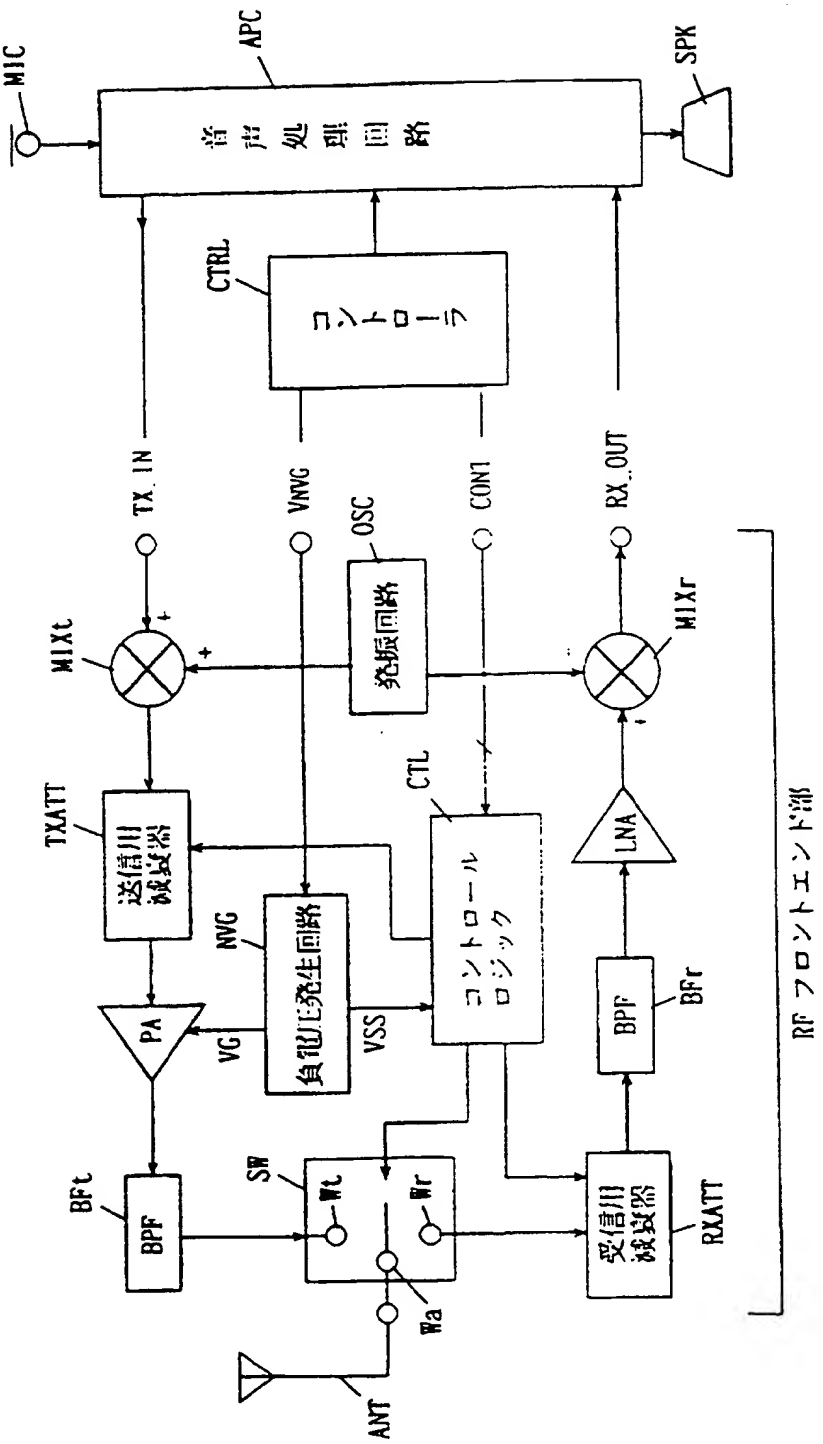

MIC
APC
SPK
音声処理回路
CTRL
コントローラ
TX_IN
VNVG
OSC
CONT
RX_OUT
MIXt
発振回路
MIXr
TXATT
送信用減衰器
CTL
LNA
NVG
コントロールロジック
負電圧発生回路
PA
VG
VSS
BPF
BFr
BFt
SW
Wt
Wr
Wa
受信用減衰器
RXATT
ANT
RFフロントエンド部

図2

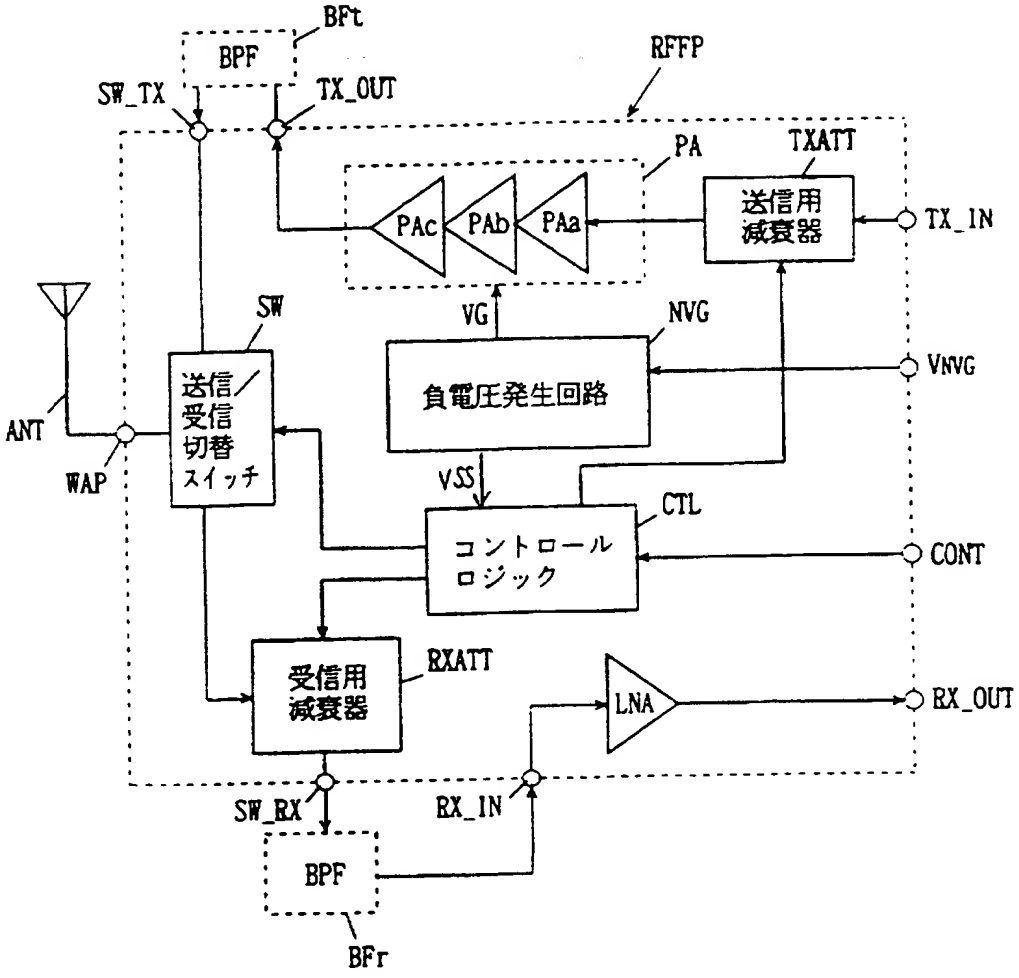

BFt
BPF
RFFP
SW_TX
TX_OUT
PA
TXATT
PAc
PAb
PAa
送信用
減衰器
TX_IN
SW
VG
NVG
送信
受信
切替
スイッチ
負電圧発生回路
VNVG
ANT
WAP
VSS
CTL
コントロール
ロジック
CONT
受信用
減衰器
RXATT
LNA
RX_OUT
SW_RX
RX_IN
BPF
BFr

図3

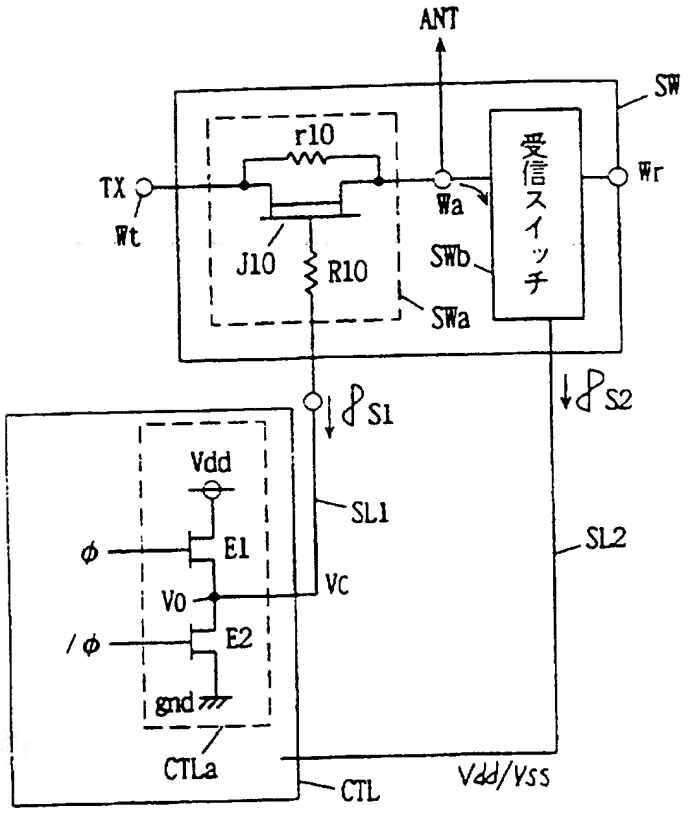

ANT
SW
r10
TX
Wt
J10
R10
Wa
SWb
SWa
受信スイッチ
Wr
S1
S2
Vdd
SL1
SL2
φ
E1
Vo
Vc
/φ
E2
gnd
CTLa
CTL
Vdd/Vss

図4

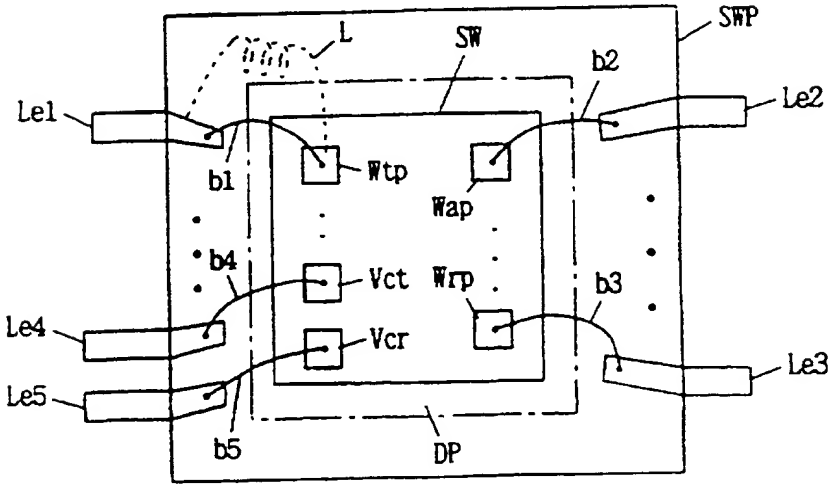

SWP
L
SW
b2
Le1
Le2
b1
Wtp
Wap
b4
Vct
Wrp
b3
Le4
Vcr
Le3
Le5
b5
DP

図5

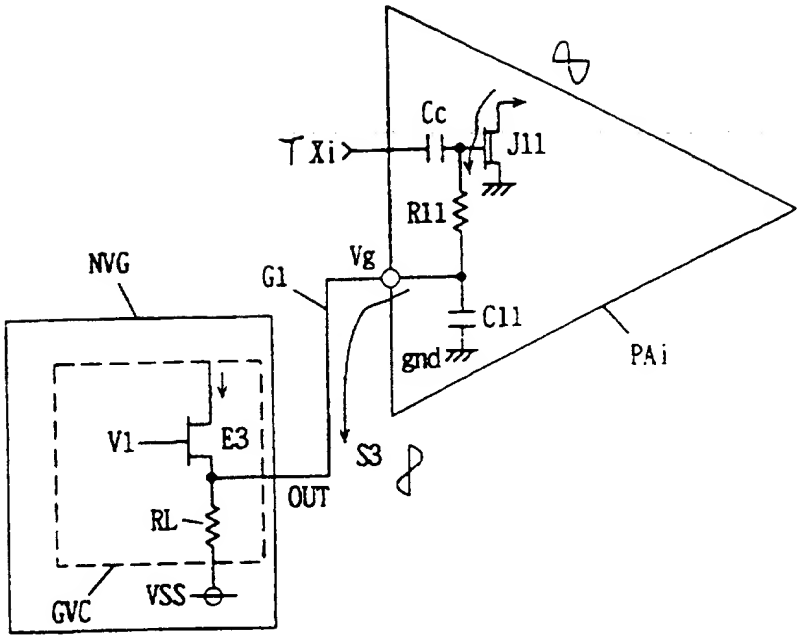

Xi
Cc
J11
R11
Vg
G1
NVG
C11
gnd
PAi
V1
E3
S3
OUT
RL
GVC
VSS

図6

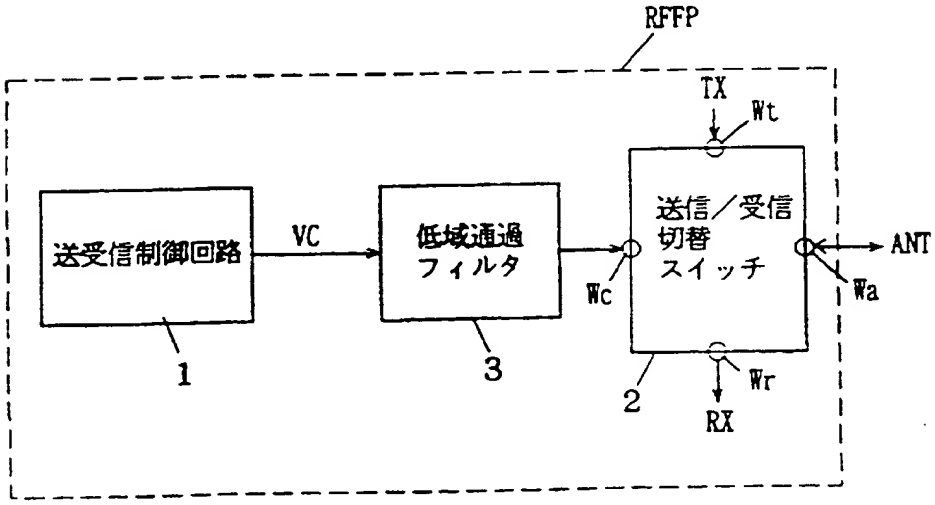

RFFP
TX
Wt
送受信制御回路
VC
低域通過
フィルタ
送信／受信
切替
スイッチ
ANT
Wc
Wa
1
3
2
Wr
RX

図7

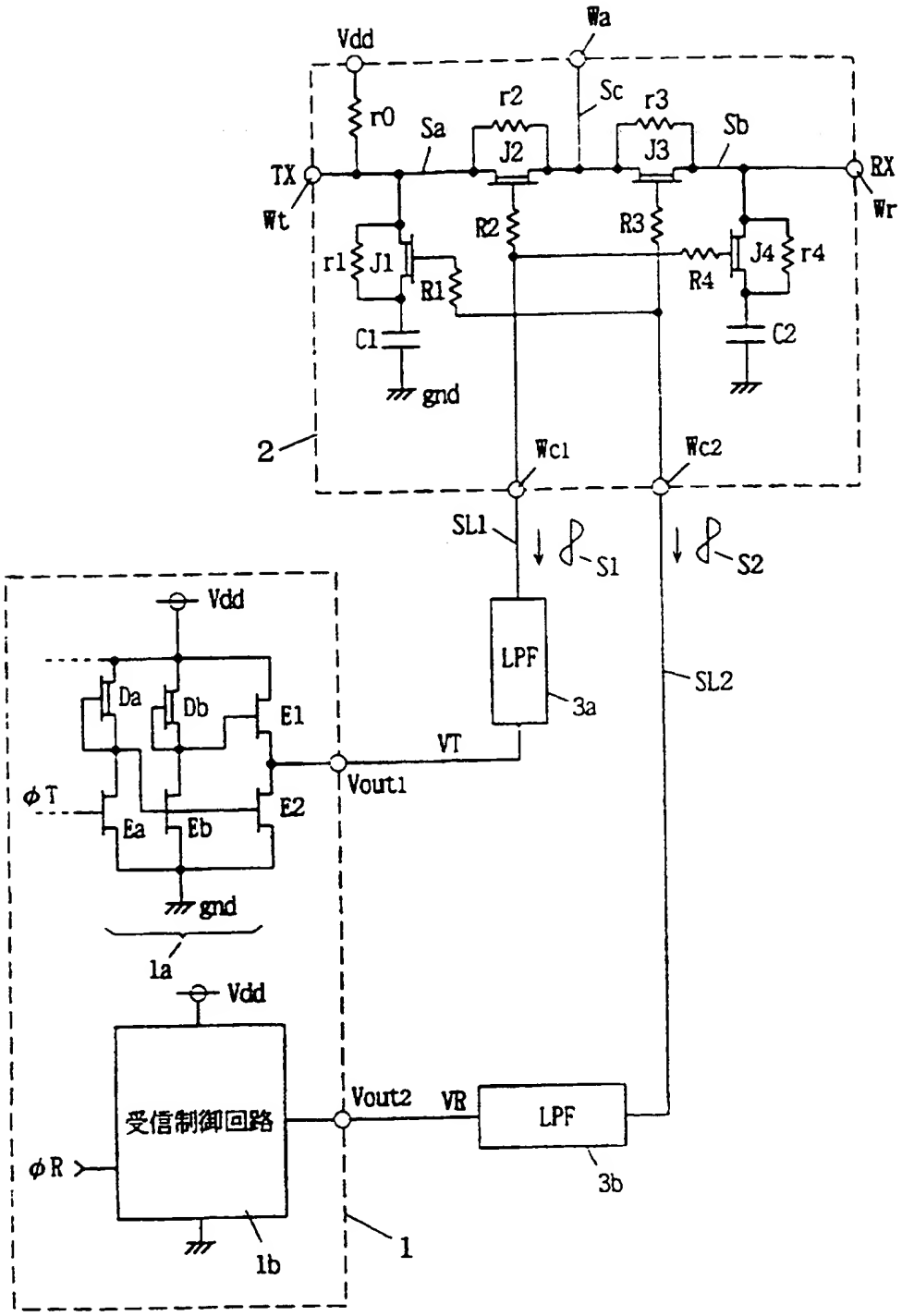

Vdd
Wa
r0
Sa
r2
Sc
r3
Sb
J2
J3
TX
RX
Wt
Wr
R2
R3
r1
J1
R1
J4
r4
R4
C1
C2
gnd
2
Wc1
Wc2
SL1
S1
S2
LPF
3a
SL2
Da
Db
E1
VT
Vout1
φT
E2
Ea
Eb
gnd
1a
Vdd
受信制御回路
Vout2
VR
LPF
3b
φR
1b
1

図８Ａ

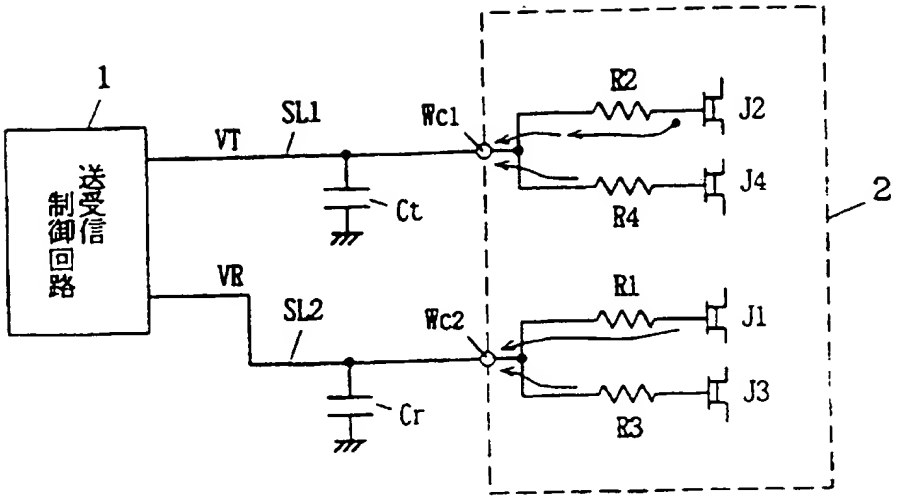

1
送受信制御回路
VT
SL1
Wc1
Ct
R2
J2
J4
R4
2
VR
SL2
Wc2
Cr
R1
J1
J3
R3

図８Ｂ

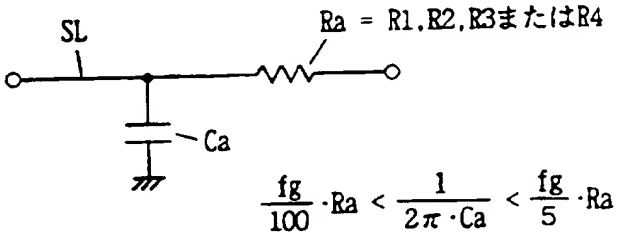

SL
Ra = R1,R2,R3またはR4
Ca
$\frac{fg}{100} \cdot Ra < \frac{1}{2\pi \cdot Ca} < \frac{fg}{5} \cdot Ra$

図８Ｃ

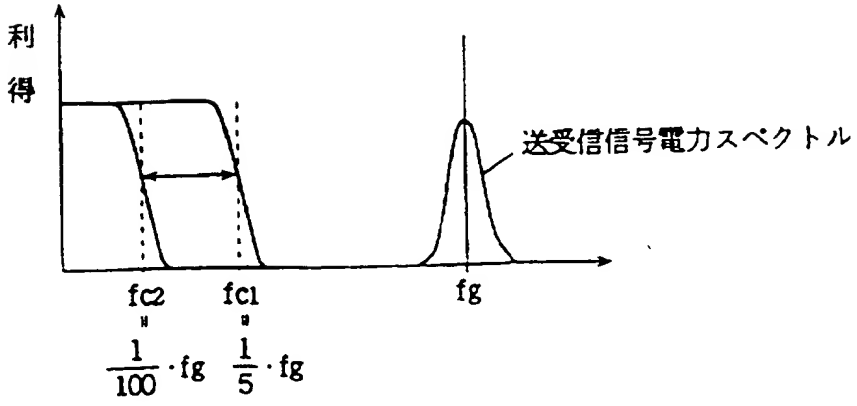

利得
送受信信号電力スペクトル
fc2
fc1
fg
$\frac{1}{100} \cdot fg$
$\frac{1}{5} \cdot fg$

図９Ａ

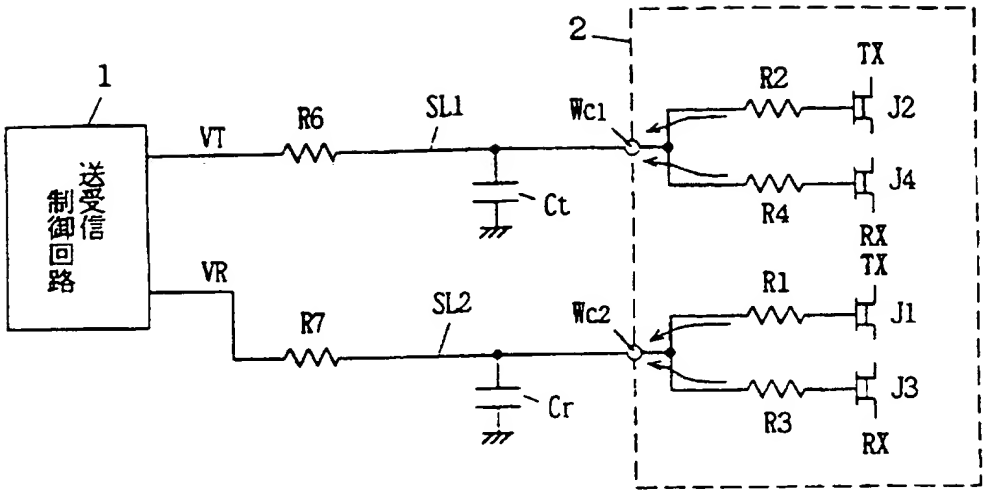

2
1
TX
R2
J2
SL1
Wc1
VT
R6
送受信制御回路
Ct
J4
R4
RX
TX
VR
R1
J1
SL2
Wc2
R7
Cr
J3
R3
RX

図９Ｂ

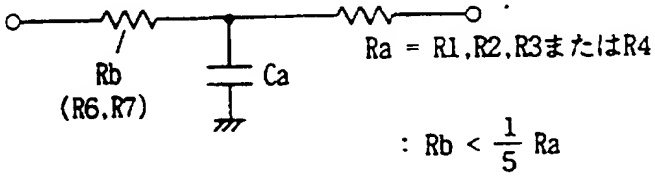

Ra = R1,R2,R3またはR4
Rb
(R6,R7)
Ca
: Rb < 1/5 Ra

図１０

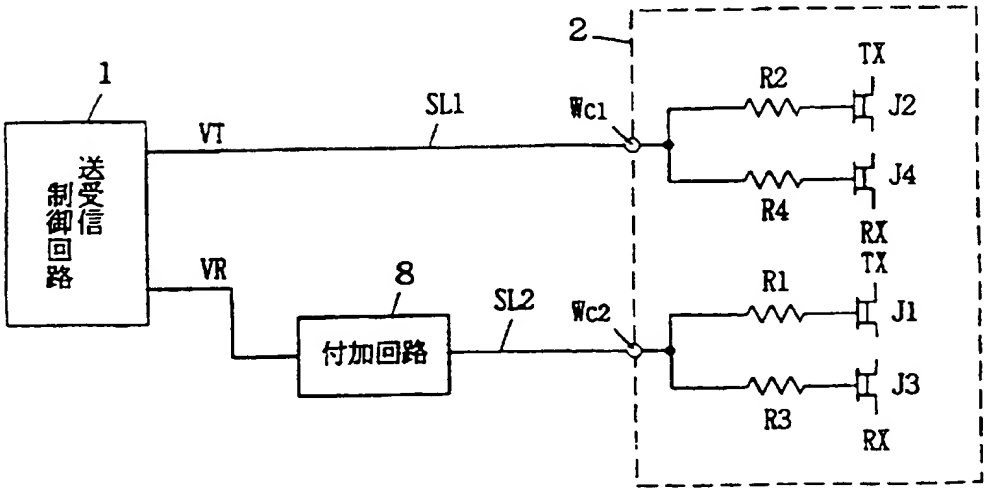

2
1
TX
R2
J2
SL1
Wc1
VT
送受信制御回路
J4
R4
RX
TX
VR
8
R1
J1
SL2
Wc2
付加回路
J3
R3
RX

図11

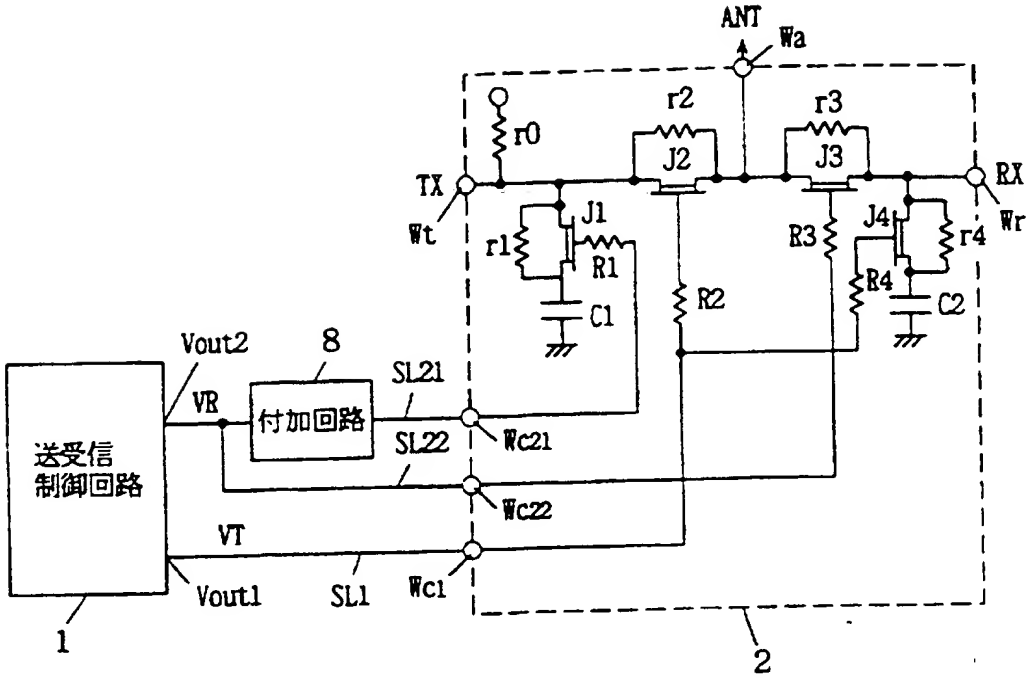

ANT
Wa
r0
r2
r3
J2
J3
TX
RX
Wt
Wr
J1
r1
R1
C1
R2
R3
J4
r4
R4
C2
Vout2
8
VR
付加回路
SL21
SL22
Wc21
Wc22
送受信
制御回路
VT
Vout1
SL1
Wc1
1
2

図13

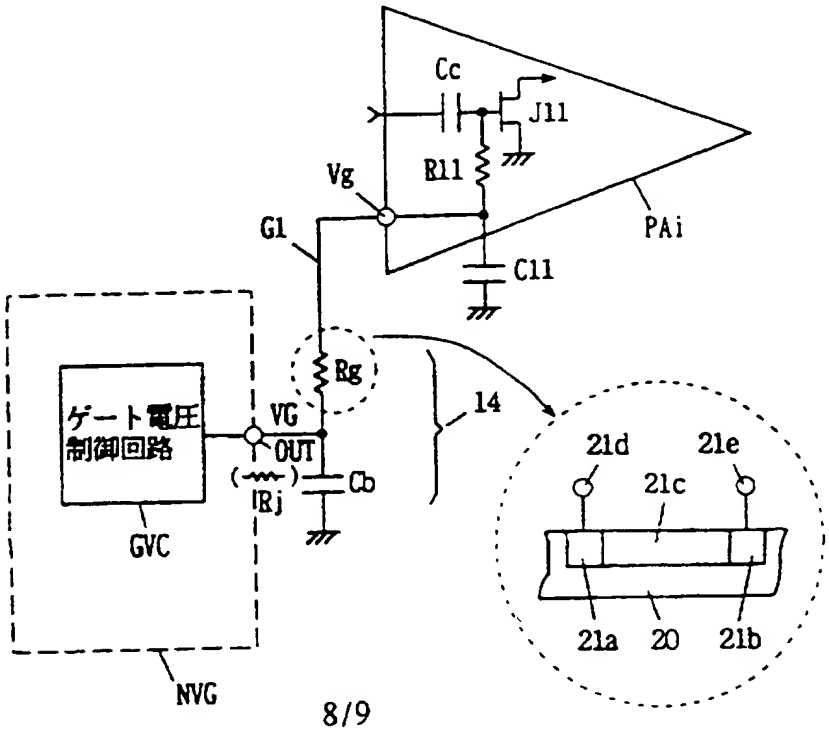

Cc
J11
R11
Vg
G1
PAi
C11
Rg
14
ゲート電圧
制御回路
VG
OUT
(Rj)
Cb
GVC
NVG
21d
21e
21c
21a
20
21b

図12A

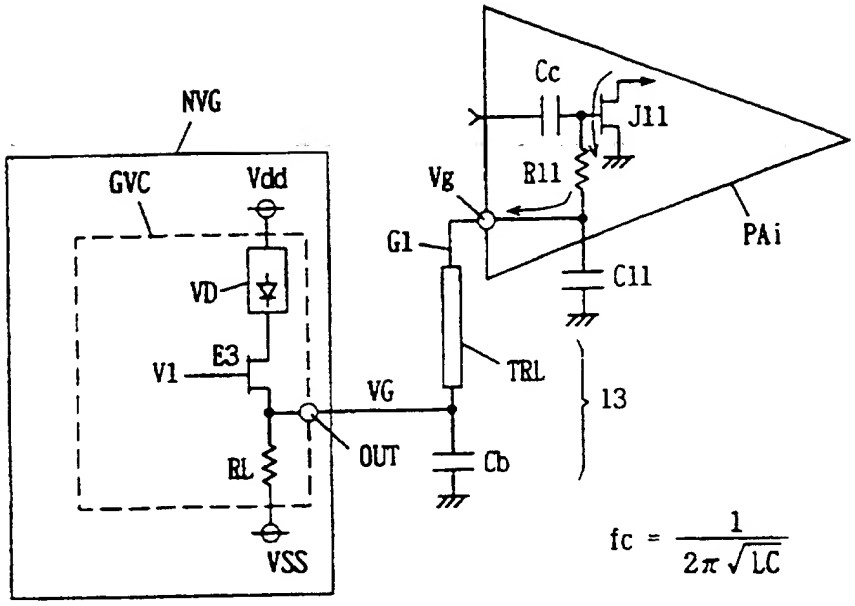


図12B

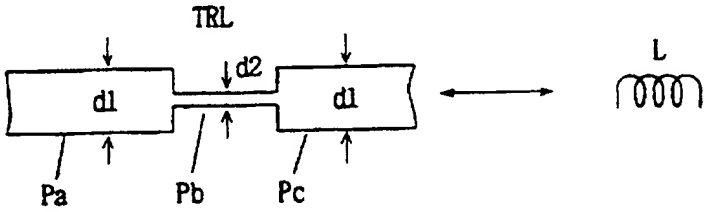
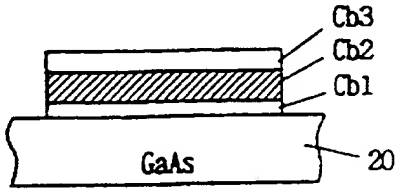


図12C



Specification

Radio-Frequency Integrated Circuit for a Radio-Frequency Wireless Transmitter-Receiver With Reduced Influence by Radio-Frequency Power Leakage

Background of the Invention

Field of the Art

The present invention relates to a radio-frequency integrated circuit for processing radio-frequency signals, and in particular to a radio-frequency integrated circuit used in a radio-frequency transmitter-receiver such as a portable telephone. More particularly, the invention relates to a radio-frequency integrated circuit having a transmission/reception multiplexing switch and a control circuit for controlling transmission/reception modes of the multiplexing switch, which are arranged in an RF front end portion for transmitting and receiving radio-frequency signals in a portable telephone, or a radio-frequency integrated circuit including a power amplifier amplifying a radio-frequency signal and a circuit producing a bias voltage for controlling a gain of the power amplifier.

Background of the Art

Recently, the market for mobile communications has been growing owing to the widespread use of extremely compact portable telephones. The mobile communications system may use an analog modulation system in which carrier waves are analog-modulated with audio signals for transmission and reception, or may use a system in which audio signals are converted into digital data, and then digital modulation of carrier waves is performed for transmission. For improving portability of such compact portable telephones, efforts have been made to reduce the size, weight and thickness thereof. For implementation of these factors, it is extremely important to reduce chip sizes of components and to enhance a functional integration.

The compact portable telephone system uses carrier waves in a frequency band of the order of gigahertz (GHz), and in the RF front end portion for transmitting and receiving such radio-frequency signals, a GaAs

IC chip including MESEFTs (Metal Semiconductor Field effect Transistors) formed using GaAs (gallium arsenide) is used as a component thereof. In GaAs technology, miniaturizing technology for GaAs has been less developed compared with silicon technology for forming MOS transistors which are formed using silicon (Si) and are used in another circuitry. Therefore, integration of the GaAs IC chips have not been developed sufficiently, and reduction in size through high integration of the components thereof have been strongly desired.

Fig. 1 schematically shows a whole structure of a portable telephone in the prior art. In Fig. 1, the portable telephone includes an RF front end portion which transmits and receives radio-frequency signals via an antenna ANT, and an audio processing circuit APC which receives a reception signal RX-OUT from the RF front end portion in a receiving operation, and performs predetermined processing on the reception signal to reproduce and apply audio signals to a speaker SPK. Audio processing circuit APC also operates, in a transmitting operation, to receive audio signals from a microphone MIC, and send the received audio signals to the RF front end portion after effecting processing, which is reverse to the processing in the receiving operation, on the audio signals. The portable telephone further includes a controller CTRL which controls operations of audio processing circuit APC and the RF front end portion.

Audio processing circuit APC includes an ADPCM codec which performs coding and decoding in accordance with, e.g., ADPCM (adaptive differential pulse code modulation) method as well as circuitry for time-division multiplexing of transmission signals and reception signals. Controller CTRL controls the switching between the transmission mode and the reception mode in audio processing circuit APC, and also performs control of the time-division multiplexing of the transmission and reception signals and other processing. Controller CTRL produces control signal CONT, which in turn includes several kinds of signals and performs instruction of the transmission/reception modes as well as control of the levels of the transmission and reception signals and other processing in the RF front end portion.

The RF front end portion further includes an oscillator circuit OSC generating a signal of a constant frequency, e.g., of 1.66 GHz, a control logic CTL which generates a signal controlling the operation of the RF front end portion in accordance with control signal CONT transferred from controller CTRL, a mixer MIXt which mixes a coded audio signal transferred from audio processing circuit APC with an oscillating signal transferred from oscillator circuit OSC, a transmission attenuator TXATT which attenuates the signal transferred from transmission mixer MIXt in accordance with the control signal transferred from control logic CTL, a negative voltage generating circuit NVG which generates a negative voltage VG in accordance with a control voltage VNVG transferred from controller CTRL, a power amplifier PA which has a gain thereof controlled with negative voltage VG transferred from negative voltage generating circuit NVG used as a bias voltage, and performs power amplification of the signal transferred from transmission attenuator TXATT, and a bandpass filter (BPF) BFt allowing passage of signals in a predetermined band out of the output signals of power amplifier PA.

Transmission mixer MIXt adds coded audio signal TX-IN transferred from audio processing circuit APC with the oscillating signal transferred from oscillator circuit OSC, to produce a radio-frequency signal suitable to transmission. Transmission attenuator TXATT reduces an amplitude of the signal transferred from mixer MIXt in accordance with a signal transferred from a radio-frequency signal intensity indicator (not shown) included in controller CTRL, and controls the level of the transmission signal.

Power amplifier PA, of which structure will be described later in more detail, includes MESFETs as its components, and receives negative voltage VG as a bias voltage for controlling the gain for operating MESFETs in a reverse bias state with the gate to source. Owing to power amplifier PA, the transmission signal is transferred via antenna ANT with a large power. The carrier wave of the transmission signal transferred from power amplifier PA is in a frequency band of about 1.9 GHz, and the transmission bandpass filter BFt allows passage of the signal in this band.

The RF front end portion further includes a transmission/reception multiplexing switch SW which multiplexes the transmission mode and the

reception mode under the control of control logic CTL.

Transmission/reception multiplexing switch SW includes a transmission signal input node Wt receiving the transmission signal from the transmission bandpass filter BFt, a transmission/reception node Wa coupled to antenna ANT, and a reception signal output node Wr. Transmission/reception node Wa is coupled electrically and selectively to one of transmission signal input node Wt and reception signal output node Wr under the control of control logic CTL.

In the portable telephone shown in Fig. 1, the transmission signal and the reception signal are in the same frequency band of approximately 1.9 GHz, and transmission and reception are switched with this transmission/reception multiplexing switch SW. As already described, audio processing circuit APC transmits and receives the transmission signal and reception signal in a time division manner and, in accordance with this time division operation, control logic CTL sets transmission/reception multiplexing switch SW to one of the transmission mode, reception mode and standby mode.

The RF front end portion further includes a reception attenuator RXATT which attenuates the reception signal transferred from reception signal output node Wr of transmission/reception multiplexing switch SW under the control of control logic CTL, a reception bandpass filter (BPF) BFr which allows passage of signals in a predetermined frequency band out of the output signals of reception attenuator RXATT, a low noise amplifier LNA which amplifies the output signal of reception bandpass filter BFr with low noises, and a reception mixer MIXr which mixes the output signal of low noise amplifier LNA with the oscillating signal from oscillator circuit OSC, and converts the radio-frequency signal into a signal in a frequency band suitable to processing of audio processing circuit APC.

Similarly to transmission attenuator TXATT, the degree of attenuation of reception attenuator RXATT is controlled by control logic CTL based on the reception signal level monitored by a personal user or control logic CTL. Reception bandpass filter BFr allows passage of signals in the frequency band of the carrier wave. Low noise amplifier LNA includes MESFETs as its components, and amplifies weak reception signals with low noises.

Reception mixer MIXr subtracts the oscillating signal of oscillator circuit OSC from the output signal of low noise amplifier LNA, and produces a reception signal (received coded audio signal) RX-OUT in the frequency band suitable to processing in audio processing circuit APC.

Fig. 2 shows a structure of the integrated circuit of the RF front end portion shown in Fig. 1. The structure of the RF front end IC shown in Fig. 2 is disclosed in "GaAs RF transceiver IC for 1.9 GHz Digital Mobile Communication Systems", Digest of Technical Papers, 1996 ISSCC, Yamamoto et al, February 10, 1996, pp. 340 - 341.

In Fig. 2, the RF front end IC includes all the components included in the RF front end portion shown in Fig. 1 except for bandpass filters BFt and BFr as well as antenna ANT. Mixers MIXt and MIXr as well as oscillating circuit OSC, which are not shown in Fig. 2, are formed in a GaAs chip or Si chip, and the chip used for them can now be selected differently. Bandpass filters BFt and BFr are arranged outside IC (chip) RFFP for accurately passing the signals in a required band, and are formed of discrete parts, and are connected to chip RFFP via terminals TX-OUT and SW-TX and terminals SW-RX and RX-TV, respectively. Thereby, the chip size of RF front end IC RFFP, and therefore the cost thereof are intended to be reduced.

Power amplifier PA includes power amplifier circuits PAa - PAc in three stages. Gains of power amplifier circuits PAa - PAc are controlled in accordance with bias voltage VG generated by negative voltage generating circuit NVG.

A negative voltage VSS applied from negative voltage generating circuit NVG to control logic CTL is used for controlling on/off of switching transistors included in transmission/receipt multiplexing switch SW. The structure for this control will be described later.

This RF front end IC is formed of a single GaAs chip. Transmission bandpass filter BFt is connected between transmission signal ports SW-TX and TX-OUT, and reception bandpass filter BFr is connected between reception ports SW-RX and RX-IN. Transmission/reception multiplexing switch SW is coupled to antenna ANT via a transmission/reception port WAP coupled to antenna ANT. Further, ports TX-IN and RX-OUT for signal

reception and transmission from and to audio processing circuit APC (see Fig. 1) as well as signal input terminals VNVG and CONT for receiving control signals are arranged.

The circuit elements included in RF front end IC RFFP shown in Fig. 2 include, as components, MESFETs formed on a GaAs substrate.

Fig. 3 shows by way of example structures of transmission/reception multiplexing switch SW and control logic CTL shown in Fig. 2. More specifically, Fig. 3 shows structures of a transmission switch SWa of transmission/reception multiplexing switch SW and an output stage CTLa controlling transmission switch SWa in control logic CTL. In the reference described previously, transmission switch SWa includes two switching transistors connected in series, but Fig. 3 shows only one of the switching transistors for simplicity reason.

In Fig. 3, transmission switch SWa includes a depletion type MESFET (Metal-Semiconductor Field effect Transistor) J10, which in turn will be referred to as a "D-MES transistor" hereinafter. D-MES transistor J10 is connected between transmission signal input node Wt and transmission/reception node Wa, and receives on its control electrode (gate) a control voltage Vc through a resistance element R10. Transmission switch SWa further includes a resistance element r10, which in turn is connected between the source and drain of D-MES transistor J10 and exhibits a high impedance in an AC (alternating current) manner. Resistance element r10 makes a connection between the source and drain of D-MES transistor J10 in a DC (direct current) manner, and holds the source and drain thereof at the same potential in the DC manner. Resistance element R10 functions as a load resistance which suppresses a current flowing through the gate of D-MES transistor J10, and also has a function of reducing an AC component.

Transmission/reception multiplexing switch SW includes a reception switch SWb arranged between transmission/reception node Wa and reception signal output node Wr. Reception switch SWb likewise includes MESFETs as its components. In the foregoing prior art reference, the MESFET included in reception switch SWb receives a control voltage changing between a positive power supply voltage Vdd and a negative voltage Vss applied from

negative voltage generating circuit NVG on its gate as a control signal, but a path for this control signal is not shown in detail (only a path SL2 is shown).

Control voltage output stage CTLa of control logic CTL includes an enhancement-type MESFET EI, which will be referred to as an "E-MES transistor" hereinafter. Enhancement-type MESFET EI is connected between a power supply node Vdd (the node and the voltage applied thereto are indicated by the same characters) and output node Vo, and receive on its gate a control signal ϕ. The control voltage output stage also includes an E-MES transistor E2 which is connected between output node Vo and a ground node gnd, and receives on its gate a control signal /ϕ. Control signals ϕ and /ϕ are signals complementary with each other.

In the transmission mode, control signal ϕ is at H-level, and control signal /ϕ is at L-level. E-MES transistor E1 is on, and E-MES transistor E2 is off so that control voltage Vc at the level of power supply voltage Vdd is applied to the gate of D-MES transistor J10 via signal line SL1 and resistance element R10. Thereby, D-MES transistor J10 is turned on so that transmission signal TX applied to transmission signal input node Wt is transferred to transmission/reception node Wa, and then is transferred to antenna ANT for transmission therefrom.

During standby or reception mode, control signal ϕ is at L-level, and control signal /ϕ is at H-level. Control voltage Vc is at the level of ground voltage gnd so that D-MES transistor J10 is turned off, and transmission signal input node Wt is isolated from transmission/reception node Wa in AC manner.

In the MESFET, the gate and the substrate region (channel region) are isolated from each other by Schottky junction. In this structure, the source/drain is coupled to the gate in the AC manner through the junction capacitance, and a radio-frequency component leaks (i.e., a radio-frequency current flows) to the gate region of the E-MES transistor. Resistance element R10 restrains this radio-frequency component. In the portable telephones, however, signals of large powers flow between ports Wt and Wa. For example, a signal of about 22 dBm flows in PHS (personal handyphone system), and a signal of about 30 dBm flows in PDC (personal digital cellular)

system. Due to such large powers, a radio-frequency component S1 leaks through the gate of D-MES transistor J10 and resistance element R10.

If the output impedance provided by E-MES transistors E1 and E2 of control voltage output stage is not sufficiently small, reflection of the radio-frequency component occurs, and control voltage Vc varies in accordance with the radio-frequency leakage component S1 so that the gate potential of D-MES transistor J10 of transmission switch SWa oscillates, and on/off thereof cannot be accurately controlled. Accordingly, the withstand power characteristics (handling power) of transmission/reception multiplexing switch SW lowers, and signals of large powers cannot be transmitted accurately.

The radio-frequency component also leaks through the MESFET included in reception switch SWb connected to port Wa. A radio-frequency component S2 flows through signal line SL2 to the control voltage generating portion of reception switch SWb, and on/off of reception switch SWb cannot be controlled accurately.

For sufficiently reducing the output impedance of output stage CTLa, MESFETs having a large gate width of 50 - 100 μm or greater must be used as E-MES transistors E1 and E2. In this case, an area occupied by output stage CTLa increases, which impedes high-density integration. If E-MES transistors E1 and E2 have a large gate width, current driving capabilities thereof must be increased for fast driving of gate capacitances thereof. For increasing such driving capabilities, it is necessary to increase the gate width of other MESFETs producing control signals ϕ and $/\phi$, which results in increase in area occupied by control logic CTL as well as increase in current consumption.

Usually, for the portable telephone including transmission/reception multiplexing switch SW, a TDMA (time-division multiple access) technology is used. Since multiple channels are allocated to the same carrier wave frequency, audio data is divided into slots, which are successively transferred or received with times shifted from each other so that conflict with another channel may be prevented. In PHS system, the carrier waves in the same frequency band (1.9 GHz) are used for transmission and reception. For these

transmission and reception, a TDD (time-division duplex) system is employed for switching in a time-division manner. In this case, however, transmission/reception multiplexing switch SW must be switched between the transmission and reception at such a high speed as several nanoseconds to hundreds of nanoseconds, and therefore E-MES transistors E1 and E2 rapidly perform the switching operation. For the fast switching operation of E-MES transistors E1 and E2 having large gate widths, the circuit generating control signals ϕ and /ϕ must rapidly change control signals ϕ and /ϕ with a large current driving capability. Accordingly, a current consumption increases in the circuit portion for generating control signals ϕ and /ϕ.

Such increase in current consumption is not preferable in portable telephones and others which operate with batteries used as an operational power supply.

Fig. 4 shows an appearance of an assembly of the RF front end portion of the portable telephone shown in Fig. 1. In Fig. 4, control logic CTL and transmission/reception multiplexing switch SW are formed on different GaAs chips, respectively. Control logic CTL and transmission/reception multiplexing switch SW which are formed on the different chips, respectively, are mounted on a board and are mutually connected. In Fig. 4, transmission/reception multiplexing switch SW is arranged on a die pad DP. Around transmission/reception multiplexing switch SW, there are arranged a pad Wtp forming transmission signal input node Wt, a pad Wap forming transmission/reception node Wa, a pad Wrp forming a reception signal output node, and pads Vct and Vcr forming control voltage input nodes. These pads Wtp, Wap, Wrp, Vct and Vcr are connected to leads Le1 - Le5 through bonding wires b1- b5, respectively. Transmission/reception multiplexing switch SW and die pad DP as well as portions of leads Le1 - Le5 are sealed in a package SWP. Leads Le1 - Le5 form external terminals for transmitting or receiving signals to or from other chips.

Bonding wires b1 - b5 have widths much larger than those of signal transmission lines included in transmission/reception multiplexing switch SW. Pads Wtp, Wap, Wrp, Vct and Vcr have sufficiently large widths. Leads Le1 - Le5 have sufficiently large widths for forming the external terminals.

Therefore, these pads, bonding wires and leads provide a large parasitic inductance L as represented by broken line in Fig. 4. In a radio-frequency band of, e.g., 1 GHz, inductance component L prevents external leakage of the radio-frequency signals ($Z = 2 \cdot \pi \cdot f \cdot L$, where f is a frequency).

Accordingly, in the structure including transmission/reception multiplexing switch SW and control logic CTL formed in the different chips, respectively, as shown in Fig. 4, no problem substantially occurs even if the radio-frequency component leaks. However, in the structure including the RF front end portion integrated in the single GaAs chip as shown in Fig. 2, the pads, bonding wires and leads shown in Fig. 4 are not present so that the radio-frequency component is not restrained, resulting in a problem that the control voltage becomes instable.

In the structure shown in Fig. 3, high inductance elements can be arranged at control signal (voltage) transmission lines SL1 and SL2. In this case, however, the chip area increases because the inductance elements formed using coils occupy a large area.

Fig. 5 schematically shows a connection between power amplifier PA and negative voltage generating circuit NVG shown in Figs. 1 and 2. More specifically, Fig. 5 shows structures of a power amplifier circuit PAi in one stage and a gate voltage control circuit GVC which generates a gate voltage Vg controlling a gain of power amplifier circuit PAi.

In Fig. 5, power amplifier circuit PAi includes a D-MES transistor J11 which receives on its gate a radio-frequency signal (transmission signal) TXi through a capacitance element Cc, and amplifies the same for applying the amplified signal to a power amplifier circuit in the next stage or an output stage, and a resistance element R11 and a capacitance element C11 which are connected in series between the gate of D-MES transistor J11 and ground node gnd. Capacitance element Cc has a function of cutting off a DC component. Capacitance element C11 is turned on in the operation frequency band of input signal TXi, to electrically connect an end of resistance element R11 to ground node gnd. Control voltage Vg is applied to a connection between resistance element R11 and capacitance element C11. Resistance element R11 biases the gate potential of E-MES transistor J11 in

accordance with control voltage Vg, and determines the operation point of D-MES transistor J11 for controlling the gain of power amplifier circuit PAi.

Gate voltage control circuit GVC of negative voltage generating circuit NVG includes an E-MES transistor E3 which receives on its gate a constant negative voltage V1, and produces control voltage Vg on an output node OUT, and a load resistance RL which is connected between output node OUT and negative voltage node VSS. E-MES transistor E3 operates in a source follower mode, and holds output node OUT at a constant potential level of (V1 - Vth), where Vth represents a threshold voltage of E-MES transistor E3. Load resistance RL has a function of pulling down the potential on output node OUT.

In power amplifier circuit PAi, capacitance element C11 is in a short-circuited state in the AC manner, and electrically couples resistance element R11 to ground node gnd in the frequency band of input signal TXi. Capacitance element C11 isolates resistance element R11 from ground node gnd in the DC manner, and resistance element R11 is supplied with control voltage Vg on its one end. Gate control voltage Vg lowers the gate voltage of D-MES transistor J11, and lowers the gain. Thereby, oscillation of the three cascaded stages of power amplifier circuits is prevented.

However, if capacitance element C11 does not short-circuit all the signals to ground node ground gnd node in the frequency band of input radio-frequency signal TXi, a radio-frequency component S3 of radio-frequency signal TXi supplied during operation of power amplifier circuit PAi or the signal amplified by transistor J11 is transmitted to gate voltage control circuit GVC via a signal line G1. Radio-frequency leakage component S3 is an AC signal. In gate voltage control circuit GVC, circuit impedance accompanied to gate voltage control circuit GVC differs for positive and negative components of radio-frequency leakage component S3 (see the foregoing reference by Yamamoto et al.). Therefore, the voltage level of control voltage Vg may vary from the desired value. This is because the radio-frequency leakage component S3 is rectified so that a performance of gate voltage control circuit GVC for holding a stable voltage in the DC manner is lowered.

The radio-frequency leakage component is restrained by the parasitic

inductance component of the bonding wires, pads and leads, if power amplifier circuit PAi and negative voltage generating circuit NVG are formed in the different chips, respectively, as shown in Fig. 4. However, the structure wherein the RF front end portion is integrated in the single chip as shown in Fig. 2 suffers from a problem similar to the foregoing problem caused by the transmission/reception multiplexing switch and the control logic.

Disclosure of the Invention

Accordingly, an object of the invention is to provide a radio-frequency integrated circuit which can operate stably even if leakage of a radio-frequency power occurs.

Another object of the invention is to provide a radio-frequency integrated circuit with a transmission/reception multiplexing switch which operates stably.

Still another object of the invention is to provide a radio-frequency integrated circuit with a power amplifier which stably amplifies a radio-frequency input signal.

Yet another object of the invention is to provide a radio-frequency integrated circuit implementing a portable telephone which operates stably with a low power consumption and a low current consumption.

The invention provides a radio-frequency integrated circuit including a field effect transistor receiving a radio-frequency input signal and transferring a signal corresponding to the radio-frequency input signal and a control voltage generating circuit applying an operation control voltage to a gate of the field effect transistor through a path other than a transmission path of the radio-frequency input signal are integrated on the same substrate, characterized in that a low pass filter is arranged in the control voltage transmission path extending from the control voltage generating circuit.

Preferably, the radio-frequency circuit is a transmission/reception multiplexing switch having a transmission mode for transferring a radio-frequency transmission signal applied to a transmission signal input node to a transmission/reception node coupled to an antenna via a first field effect transistor, and a reception mode for transferring a radio-frequency reception signal applied to the transmission/reception node to a reception signal output

node via a second field effect transistor, and operating in the operation mode determined by driving the first and second field effect transistors to the on/off state by the control voltage applied from the control voltage generating circuit.

Alternatively, the radio-frequency circuit can be a power amplifier amplifying the radio-frequency input signal by a field effect transistor, wherein the control voltage generated by the control voltage generating circuit determines a gate voltage of the field effect transistor for determining a gain of the power amplifier.

Owing to provision of the low pass filter at the control voltage transmission path, the low pass filter can absorb a radio-frequency leakage component of the radio-frequency signal of a high power, which may leaks from the radio-frequency circuit through the field effect transistor into the control signal transmission path. Therefore, the control voltage can be stably held at the constant level, and the stable operation can be ensured.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Fig. 1 is a diagram schematically showing a whole construction of a conventional portable telephone.

Fig. 2 schematically shows a structure including an RF front end portion shown in Fig. 1 and integrated in a single chip.

Fig. 3 schematically shows structures of a transmission/reception multiplexing switch and a transmission/reception multiplexing portion thereof shown in Figs. 1 and 2.

Fig. 4 schematically shows an assembly of the transmission/reception multiplexing switch in the prior art.

Fig. 5 schematically shows a structure of a connection between a power amplifier and a negative voltage generating circuit shown in Figs. 1 and 2.

Fig. 6 schematically shows a structure of an embodiment 1 of the invention.

Fig. 7 shows a specific structure according to an embodiment 1 of the

invention.

Fig. 8 shows a first modification of the embodiment 1 of the invention.

Fig. 9 shows a second modification of the embodiment 1 of the invention.

Fig. 10 shows a third modification of the embodiment 1 of the invention.

Fig. 11 shows a fourth modification of the embodiment 1 of the invention.

Figs. 12A - 12C schematically show a structure of a radio-frequency integrated circuit according to an embodiment 2 of the invention.

Fig. 13 shows a modification of the embodiment 2 of the invention.

The Best Mode for Carrying Out the Invention

Fig. 6 schematically shows a structure of a radio-frequency integrated circuit of an embodiment 1 of the invention. In Fig. 6, an RF front end integrated circuit (chip) RFFP includes a transmission/reception control circuit 1 which produces a control voltage VC designating an operation mode among a transmission mode, a reception mode and a standby mode; a transmission/reception multiplexing switch 2 provided corresponding to a radio-frequency circuit and operating in the transmission/reception or standby mode in accordance with control voltage VC transferred from transmission/reception control circuit 1, and a low pass filter 3 provided at a signal line transmitting control voltage VC between transmission/reception control circuit 1 and transmission/reception multiplexing switch 2.

Transmission/reception control circuit 1 is included in control logic CTL shown in Figs. 1 and 2, and produces control voltage VC at a required voltage level in accordance with an operation mode instructing signal transferred from controller CTRL shown in Fig. 1.

Transmission/reception multiplexing switch 2 includes transmission signal input node Wt receiving radio-frequency transmission signal TX, transmission/reception node Wa coupled to antenna ANT, reception signal output node Wr outputting a radio-frequency reception signal, and a control voltage input node Wc receiving control voltage VC.

Low pass filter 3 cuts off a radio-frequency leakage component flowing from transmission/reception multiplexing switch 2 to transmission/reception control circuit 1. Transmission/reception multiplexing switch 2 applies

transmission signal TX, which is applied to transmission signal input node Wt, to transmission/reception node Wa when the transmission mode is designated in accordance with the voltage level of control voltage VC. In the reception mode, the transmission/reception multiplexing switch 2 outputs the radio-frequency reception signal, which is applied to transmission/reception node Wa, through reception signal output node Wr. A reception signal RX transferred from transmission/reception multiplexing switch 2 is applied to reception attenuator RXATT shown in Fig. 2.

As shown in Fig. 6, low pass filter 3 is arranged at a signal line transmitting control voltage VC from transmission/reception control circuit 1, whereby a radio-frequency component, which may leak when transmission/reception multiplexing switch 2 sends the transmission signal of a high power therefrom, can be prevented from reaching transmission/reception control circuit 1. Therefore, control voltage VC at the constant voltage level can be stably applied to transmission/reception multiplexing switch 2.

Fig. 7 shows specific structures of transmission/reception control circuit 1 and transmission/reception multiplexing switch 2 shown in Fig. 6. In Fig. 7, transmission/reception control circuit 1 includes a transmission control circuit 1a which produces reception control voltage VT for activating/deactivating the transmission mode in accordance with a transmission mode instructing signal ϕT, and a reception control circuit 1b which produces reception control voltage VR in response to a reception mode instructing signal ϕR. Transmission control circuit 3a and reception control circuit 1b have similar structures, and therefore Fig. 7 shows only the structure of transmission control circuit 1a.

Transmission control circuit 1a includes a D-MES transistor (i.e., depletion-type MES transistor) Da which has one conduction node to power supply node Vdd (the node and the voltage applied thereto are indicated by the same characters), and a gate connected to the other conduction node, an E-MES transistor Ea which has one conduction between D-MES transistor Da and ground node gnd, and receives transmission mode instructing signal ϕT on its gate, a D-MES transistor Db which has one conduction node connected

to power supply node Vdd and a gate connected to the other conduction node, an E-MES transistor Eb which is connected between D-MES transistor Db and ground node gnd and has a gate connected to the gate of D-MES transistor Da and the other conduction node thereof, an E-MES transistor E1 which is connected between power supply node Vdd and output node Vout1 and has a gate connected to the gate of D-MES transistor Db, and an E-MES transistor E2 which is connected between output node Vout1 and ground node gnd and has a gate connected to the gate of D-MES transistor Da and the other conduction node thereof.

Power supply voltage Vdd is about 3 V. D-MES transistors Da and Db operate as load elements, and these transistors Da and Db and E-MES transistors Ea and Eb form two cascaded inverters.

When transmission mode instructing signal ϕT is at H-level, E-MES transistor Ea is on, and the gate and the other conduction node of D-MES transistor Da are at the level of ground potential gnd so that E-MES transistor Eb is off. Thereby, E-MES transistor E1 receives on its gate the signal at H-level and is turned on, and E-MES transistor E2 receives on its gate the signal at L-level and is turned off. In this state, control voltage VT transferred from output node OUT1 is at H-level of power supply voltage Vdd.

When transmission mode instructing signal ϕT is at L-level, E-MES transistor E1 is off and E-MES transistor E2 is on, so that control voltage VT is at L-level of ground potential gnd.

In reception control circuit 1b, when reception mode instructing signal ϕR is active (H-level), control voltage VR transferred from output node Vout is at H-level of power supply potential Vdd. When reception mode instructing signal ϕR is inactive (L-level), control voltage VR is at L-level of ground potential gnd.

In the communication mode, switching between these operation mode instructing signals ϕT and ϕR is performed at high speed in a time-division manner. In the standby mode, these operation mode instructing signals ϕT and ϕR are inactive.

Transmission/reception multiplexing switch 2 includes a D-MES transistor J2 which is connected between transmission signal input node Wt

and transmission/reception node Wa and receives, on its gate, transmission control voltage VT from transmission control circuit 1a through resistance element R2, a D-MES transistor J1 which is connected between ground node gnd and a signal line Sa coupled to transmission signal input node Wt and receives, on its gate, reception control voltage VR from reception control circuit 1b through resistance element R1, a D-MES transistor J3 which is connected between transmission/reception node Wa and reception signal output node Wr and receives, on its gate, control voltage VR from reception control circuit 1b through resistance element R3, and a D-MES transistor J4 which is connected between reception signal output node Wr and ground node gnd and receives, on its gate, control voltage VT from transmission control circuit 3a through resistance element R4.

A signal line Sb is arranged between D-MES transistor J3 and reception signal output node Wr, and a signal line Sc is arranged between transmission/reception node Wa and D-MES transistors J2 and J3.

Transmission/reception multiplexing switch 2 includes a resistance element r0 connected between signal line Sa and power supply node Vdd, a resistance element r1 for connecting the source and the drain of D-MES transistor J1 in the DC manner, a capacitance element C1 connected between resistance element r1 and D-MES transistor J1, and ground node gnd, a resistance element r2 connected between the source and drain of D-MES transistor J2, a resistance element r3 connected between the source and drain of D-MES transistor J3, a resistance element r4 connected between the source and drain of D-MES transistor J4, and a capacitance element C2 connected between resistance element r4 and D-MES transistor J4, and the ground node gnd.

Transmission signal TX and reception signal RX are transmitted through transmission lines having a characteristic impedance of about 50 Ω. Resistance elements r0 - r4 have resistance values of the order of kilo-ohms, and provide isolation in the AC manner between the sources and drains of D-MES transistors J1 - J4 respectively in the frequency band of transmission signal TX and reception signal RX. Signal line Sa is coupled to power supply potential Vdd via resistance element r0, and therefore signal lines Sb and Sc

are pulled up to the level of power supply potential Vdd owing to coupling in the DC manner by resistance elements r2 and r3. Likewise, the sources and the drains of D-MES transistors J1 and J4 are coupled in the DC manner by resistance elements r1 and r4, respectively, and are pulled up to the level of power supply potential Vdd.

Resistance elements R1 - R4 likewise have resistance values of the order of kilo-ohms, and suppress leakage of radio-frequency components during transmission and reception of the radio-frequency signal.

Capacitance elements C1 and C2 are made conductive in the frequency band of the transmission signal and reception signal, and thereby prevent interference between the transmission signal and the reception signal.

Low pass filter 3 includes low pass filters (LPFs) 3a and 3b, which are arranged between output nodes Vout1 and Vout2 of transmission/reception control circuit 1 and control voltage input nodes Wc1 and Wc2 of transmission/reception selector switch 2, respectively. Now, operation of transmission/reception selector switch 2 shown in Fig. 7 will be described below.

In the standby mode, control voltages VT and VR applied to nodes Wc1 and Wc2 are at L-level of ground potential gnd. In this state, D-MES transistors J1 - J4 are off. More specifically, all signal lines Sa, Sb and Sc are pulled up to the level of power supply potential Vdd owing to resistance element r0, and the sources and drains of D-MES transistors J1 and J4 are held at the level of power supply potential Vdd by resistance elements r1 and r4, respectively. In each of D-MES transistors J1 - J4, therefore, a deep reverse bias state is established between the gate and the source, and even the depletion mode transistors are reliably turned off by the control voltages VT and VR at the ground potential level.

In the transmission mode, control voltage VT is at H-level of power supply potential Vdd, and reception control voltage VR maintains the level of ground potential gnd. In this state, D-MES transistors J2 and J4 are on, and D-MES transistors J1 and J3 are off. Owing to the on state of D-MES transistor J4, a radio-frequency component which leaks through D-MES transistor J3 and appears on signal line Sb is discharged to ground node gnd

so that the transmission signal is prevented from being transmitted through reception signal output node Wr.

Resistance element r1 cuts off transmission signal TX by its relatively large resistance value, and prevents transmission signal TX, which appears on signal line Sa, from being discharged to ground node gnd through capacitance element C1.

The transmission signal TX is a high power signal amplified by the power amplifier. Due to the high power of transmission signal TX, a radio-frequency component may leak to the gate of D-MES transistor J2 through a junction capacitance, and may not be absorbed by resistance element R2. Even in this case, radio-frequency component S1 is absorbed by low pass filter (LPF) 3a, and control voltage VT is stably held at the constant voltage level by E-MES transistors E1 and E2. (The radio-frequency leakage component itself changes the potentials on the gate and source of a transistor in the same direction, and does not significantly affect the switching characteristics.) Thereby, the transmission can be performed stably even in the high power operation, and the withstand power characteristics (i.e., handling power) is improved.

Leakage of the radio-frequency component due to transmission signal TX of the high power may also occur at the junction capacitance of the gate of D-MES transistor J1, and may not be absorbed by resistance element R1. Even in this case, low pass filter (LPF) 3b provided at signal line SL2 prevents radio-frequency leakage component S2 from affecting control voltage VR transferred from reception control circuit 1b so that control voltage VR is reliably held at the ground potential level, and D-MES transistors J3 and MES transistor J1 are maintained off.

When radio-frequency transmission signal TX is transferred to signal line Sc, a radio-frequency component thereof may leak through the gate of D-MES transistor J3, and may not be absorbed by resistance element R3. Even in this case, low pass filter 3b absorbs the radio-frequency leakage component. Further, the radio-frequency component may leak to signal line Sb through D-MES transistor J3 (the radio-frequency component is restrained by resistance element r3), and the radio-frequency leakage component on signal line Sb

may be transferred to signal line SL1 through the gate of D-MES transistor J4 and resistance element R4. Even in this case, low pass filter 3a absorbs the radio-frequency leakage component. In Fig. 7, the combined components on signal lines SL1 and SL2 formed of the radio-frequency leakage components transferred through these D-MES transistors are indicated by characters S1 and S2, respectively.

MESFET must operate with the gate to source/drain kept in a reverse bias state. Resistance elements r1 - r4 and R1 - R4 have functions of cutting off the radio-frequency components as well as functions of operating D-MES transistors J1 - J4 each with the gate to source/drain kept in a reversedly biased state.

In the transmitting operation, radio-frequency components S1 and S2 may leak to control voltage transmission lines SL1 and SL2 due to radio-frequency transmission signal TX of a high power. Even in this case, low pass filters 3a and 3b absorb radio-frequency leakage components S1 and S2, respectively. Therefore, it is not required to increase the gate widths of E-MES transistors E1 and E2 at the output stages of control circuits 1a and 1b. Accordingly, it is possible to reduce the current driving capabilities and therefore the gate widths of MES transistors Da, Db, Ea and Eb controlling on/off of E-MES transistors E1 and E2 so that the current consumptions and occupying areas of control circuits 1a and 1b can be reduced. Consequently, an area occupied by transmission/reception control circuit 1 can be reduced. Accordingly, transmission/reception multiplexing switch 2 and transmission/reception control circuit 1 can be integrated on a single chip without increasing the chip area.

Owing to employment of the MESFETs in the depletion mode, the on-state thereof can be made deeper as compared to MESFETs in the enhancement mode so that the radio-frequency signal can be efficiently transmitted without a signal loss.

In the reception mode, control voltage VT is at L-level, and control voltage VR is at H-level. In this state, D-MES transistors J2 and J4 are off, and D-MES transistors J1 and J3 are on. The radio-frequency component on signal line Sa is discharged to ground node gnd through D-MES transistor J1

and capacitance element C1, and the transmission signal component is transferred to transmission/reception node Wa through signal line Sc so that interference between the transmission signal and the reception signal is prevented. The reception signal applied to transmission/reception node Wa has a smaller power than transmission signal TX, so that may be amplified by the low noise amplifier shown in Fig. 1 (although the reception signal may have a high power at a position near the transmission source). In this state, even if the radio-frequency component leaks through the gates of D-MES transistors J1 - J4 to signal lines SL1 and SL2, the radio-frequency leakage component is absorbed by low pass filters 3a and 3b so that, in the receiving operation, control voltages VT and VR are stably held at the constant voltage level similarly to the transmitting operation, and the accurate receiving operation is ensured.

For high-density integration, low pass filters 3a and 3b are not implemented using coils such as choke coils dedicated to radio-frequency cut-off, and are formed of the circuits including resistance elements R and capacitance elements C, whereby low pass filters 3a and 3b do not occupy a large area, and does not impede the high-density integration.

[Modification 1]

Fig. 8A shows a structure of a first modification of the embodiment 1 of the invention. In Fig. 8A, capacitance elements Ct and Cr are arranged for signal lines SL1 and SL2 in parallel with them, respectively. In transmission/reception multiplexing switch 2, gates of D-MESFETs J1 - J4 are connected to resistance elements R1 - R4, respectively. Resistance elements R2 and R4 are connected to signal line SL1, and resistance elements R1 and R3 are connected to signal line SR2. Resistance elements R1 - R4 are used as resistance components of the low pass filters. More specifically, as shown in Fig. 8B, capacitance Ca (Ct or Cr) is arranged between each signal line SL (SL1 or SL2) and ground node gnd, and resistance element R2 or R4, or resistance element R1 or R3 is used for resistance element Ra. When viewed from the gate of MES transistor J2, the resistance value of resistance element R4 is sufficiently larger than that of transmission line SL1 and can be ignored, and the converse also hold.

It is necessary to provide only capacitance elements Ct and Cr as the low pass filters, and additional resistance elements are not required so that the area occupied by the low pass filters can be made small.

In the low pass filter using the RC circuit, the cut-off frequency fc is expressed by the following formula:

$$fc = 1/(2 \cdot \pi \cdot Ca \cdot Ra)$$

The resistance value of resistance element Ra and the capacitance value of capacitance element Ca are so determined as to satisfy the relationship expressed by the following unequation:

$$1/2 \cdot \pi \cdot Ca < fg \cdot Rg/5; \quad fc < fg/5$$

Thus, cut-off frequency fc of the low pass filter is restricted to be lower than 1/5 times operation frequency fg. Operation frequency fg is the frequency band of the transmission signal TX and reception signal RX, and is e.g., 1.9 GHz. In receivers such as a portable telephone, the power spectrum is concentrated on and around the band of carrier wave (operation) frequency fg.

As shown in Fig. 8C, resistance values Ra of resistance elements R1 - R4 as well as capacitance values Ca of capacitance elements Ct and Cr are determined to satisfy the relationship expressed by the above unequation, whereby the radio-frequency leakage component can be reliably cut off. In this case, capacitance values Ca of capacitance elements Ct and Cr may be relatively small, and therefore the area occupied by the capacitance elements can be reduced. By employing the low pass filters of which cut-off frequency fc (= fc1) is smaller than 1/5 times operation frequency (carrier wave frequency band) fg, the radio-frequency signals can be reliably passed through low pass filters even when transmission/reception control circuit 1 performs fast switching between control voltages VT and VR. Therefore, D-MESFETs J1 - J4 can perform the switching operation so that the communications can be performed in a time-division manner by performing fast switching between the transmission and reception.

In this case, resistance values Ra of resistance elements R1 - R4 and capacitance values Ca of capacitance elements Ct and Cr are determined to satisfy the following relationship:

$$fg \cdot Ra/100 < 1/2 \cdot \pi \cdot Ca < fg \cdot Ra/5$$

Thereby, it is not necessary to increase excessively capacitance values of capacitance elements Ct and Cr for the low pass filters, and therefore the area occupied by the capacitance elements can be reduced. In this case, even if transmission/reception control circuit 1 performs switching between control voltages VT and VR at a high speed, cut-off frequency fc2 shown in Fig. 8C allows passing of the signal in a band from a few nanoseconds to hundreds of nanoseconds so that fast operation can be sufficiently achieved.

[Modification 2]

Fig. 9A shows a structure according to a second modification of the embodiment 1 of the invention. In the structure shown in Fig. 9A, a resistance element R6 is arranged between capacitance element Ct and the control voltage output node of transmission/reception control circuit 1, and a resistance element R7 is arranged on signal line SL2 between transmission/reception control circuit 1 and capacitance element Cr. Structures other than the above are the same as those shown in Fig. 8A, and corresponding portions bear the same reference numerals.

In the structure shown in Fig. 9A, a T-shaped low pass filter is arranged as shown in Fig. 9B that is an equivalent circuit diagram of the structure. In this structure, the impedance of resistance element Rb viewed from capacitor Ca can be higher than that in the structure of Figs. 8A and 8B so that a filtering performance of the low pass filter formed of resistance element Rb and capacitor Ca can be improved. Therefore, the filtering performance similar to that in the structure of Figs. 8A and 8B can be achieved even when the capacitance value of capacitor Ca is set to a smaller value. Accordingly, the area occupied by the capacitor can be reduced. Resistance elements R6 and R7 are made of diffusion resistances, which are formed by implanting impurity into impurity regions at the surface of GaAs substrate, and the required resistance values can be achieved with small occupied areas. Meanwhile, the capacitance elements are implemented by forming parallel electrode layers on the surface of the substrate.

Although resistance elements R6 and R7 are employed, the area occupied by the capacitance elements can be reduced more than the increase by resistance elements R6 and R7. Consequently, the area occupied by the

low pass filters can be reduced.

The resistance values of resistance elements Ra and Rb are so determined as to satisfy the following relationship:

$Rb < Ra/5$

The radio-frequency leakage component flows from transmission/reception multiplexing switch 2 toward transmission/reception control circuit 1 through signal lines SL1 and SL2. It can be considered that the T-shaped structure of the low pass filter is equivalent to the structure including two cascaded low pass filters. Accordingly, by employing resistance element Ra larger in resistance value than resistance element Rb, the leakage component can be sufficiently absorbed owing to the transmission parameter $(1 + j \cdot \omega \cdot Ca \cdot Ra)$ of the RC low pass filter formed of resistance element Ra and capacitance element Ca. Therefore, even if the resistance value of resistance element Rb is small, the radio-frequency leakage component can be sufficiently absorbed at a portion near the transmission path thereof.

The resistance value of resistance element Rb can be small, and the area occupied by resistance element Rb can be reduced (i.e., the required resistance value can be achieved with a small diffusion region). Also, the area occupied by capacitance element Ca can be reduced, and the low pass filter occupying a small area can be achieved.

[Modification 3]

Fig. 10 shows a structure according to a third modification of the embodiment 1 of the invention. In the structure shown in Fig. 10, an additional circuit 8 for absorbing the radio-frequency leakage component is arranged for signal line SL1 transmitting reception control voltage VR. Additional circuit 8 may be the low pass filter (LPF) shown in Fig. 7, or may be simply the capacitance element shown in Fig. 8A. Also, it may be a combination of capacitance element Cr and resistance element R7 shown in Fig. 9A.

Reception control voltage VR is applied from control voltage input node Wc2 through resistance elements R1 and R3 to the gates of D-MES transistors J1 and J3 which are turned off in the transmission mode, respectively. In the transmission mode, D-MES transistors J1 and J3 must be reliably off. If

D-MES transistors J1 and J3 were weakly on, transmission signal TX would be discharged to the ground potential level through D-MES transistor J1, and would also be discharged to the ground potential level through D-MES transistor J3 and D-MES transistor J4 that is on in the transmission mode, resulting in a large loss of the transmission signal. For improving the withstand power characteristics in the transmission mode, it is particularly necessary that D-MES transistors J1 and J3, which are to be off in the transmission operation, accurately receive the voltages at L-level at the respective gates and thereby are reliably kept off.

Owing to provision of additional circuit 8 on reception control voltage transmission line SL2 as shown in Fig. 10, additional circuit 8 can absorb the radio-frequency leakage component even if it flows to signal line SL2 through D-MES transistors J1 and J3 which are to be off in the transmission mode. Thereby, D-MES transistors J1 and J3 can be reliably kept off so that discharging of transmission signal TX through transistors J1 and J3 can be prevented. At this time, transmission signal TX may partially leak to signal line SL1 through D-MES transistors J2 and J4. Even in this case, D-MES transistors J2 and J4 are in the depletion mode and are in the strong on state. Therefore, an influence which is exerted on the loss of transmission signal TX by D-MES transistors J2 and J4 is smaller than that by the discharging of transmission signal TX through D-MES transistors J1 and J3.

Accordingly, an effect similar to that of the foregoing embodiment shown in Fig. 7 can be achieved by provision of additional circuit 8 for absorbing the radio-frequency component on the signal line SL2 transmitting reception control voltage VR.

[Modification 4]

Fig. 11 shows a structure according to a fourth modification of the embodiment 1 of the invention. The signal line for transmitting reception control voltage VR is divided into a signal line SL21 which transmits control voltage VR to the gate of D-MES transistor J1 of transmission/reception multiplexing switch 2, and a signal line SL22 which transmits control voltage VR to the gate of D-MES transistor J3. Signal lines SL21 and SL22 are coupled to control voltage input nodes Wc21 and Wc22 of

transmission/reception multiplexing switch 2, respectively. Transmission control voltage VT is coupled to control voltage input node Wc1 of transmission/reception multiplexing switch 2 through signal line SL1. Control voltage input node Wc1 is coupled to the gates of D-MES transistors J2 and J4 through resistance elements R2 and R4, respectively.

Additional circuit 8 is provided only for signal line SL21. Additional circuit 8 has the structure in any one of the foregoing embodiments.

In the transmission mode, when D-MES transistor J1 is turned on, transmission signal TX is discharged to the ground potential level through D-MES transistor J1 and capacitance element C1 to increase the loss of the transmission signal TX so that the transmission signal of a high power cannot be transferred to antenna ANT. Thus, it is D-MES transistor J1 that exerts the largest influence on the loss of the transmission signal TX. Transmission signal TX is also transferred to D-MES transistor J3. When viewed from D-MES transistor J2, however, the impedance with respect to transmission/reception input node Wa is much smaller than the impedance with respect to D-MES transistor J3. Therefore, a major part of transmission signal TX transferred from D-MES transistor J2 is transferred to antenna ANT through transmission/reception node Wa.

When viewed from transmission signal input node Wt, if the gate potential of D-MES transistor J1 may rise and the impedance of D-MES transistor J1 may decrease, the signal transmission path including D-MES transistor J1 cannot be ignored with respect to the signal transmission path including D-MES transistor J2. Therefore, transmission signal TX is discharged through D-MES transistor J1 and capacitance element C1, resulting in a large power loss of transmission signal TX. In this transmission mode, therefore, it is D-MES transistor J1 that exerts the largest influence on the loss of transmission signal TX. Owing to provision of additional circuit 8 for signal line SL21 transmitting control voltage VR for D-MES transistor J1, D-MES transistor J1 can have the gate voltage kept constant in the DC manner, and can reliably keep the off state even when the radio-frequency leakage occurs in D-MES transistor J1. Thereby, the loss of transmission signal TX is prevented. Accordingly, transmission signal TX of

the high power can be transmitted without an increased large transmission loss, and lowering of the withstand power characteristics can be prevented similarly to the foregoing structures of the embodiment.

According to the embodiment 1 of the invention, as described above, in the RF front end portion including transmission/reception control circuit 1 and transmission/reception multiplexing switch 2 integrated on the same substrate, the low pass filter for absorbing the radio-frequency leakage component is arranged at the control voltage transmission path between the transmission/reception control circuit 1 and the transmission/reception multiplexing switch 2. Even if the radio-frequency leakage component occurs, therefore, it is possible to suppress an influence, which may be exerted on the control voltage level by the radio-frequency leakage component, and the control voltage which is at the constant voltage level in DC manner can be transmitted to transmission/reception multiplexing switch 2. Thus, without an influence by the radio-frequency leakage component, the transistor to be off can be reliably kept off, and the transistor to be on can be reliably kept on. Accordingly, lowering of the handling power characteristics can be prevented.

For absorbing the radio-frequency leakage component, the resistance elements and the capacitance elements are used, and no coil is used. Therefore, it is possible to provide a filter for absorbing the radio-frequency leakage component with a reduced occupying area. Further, by absorbing the radio-frequency leakage component, it is not necessary to increase the gate widths of the MES transistors which are the components of transmission/reception control circuit 1 so that the occupying area and current consumption of the transmission/reception control circuit 1 can be reduced.

[Embodiment 2]

Fig. 12A shows a structure of a radio-frequency integrated circuit of an embodiment 2 of the invention. In Fig. 12A, a low pass filter 13 is arranged between gate voltage output node OUT of gate voltage control circuit GVC included in negative voltage generating circuit NVG and control voltage input node Vg of power amplifier circuit PAi, i.e., the radio-frequency circuit. Power amplifier circuit PAi has the same structure as the power amplifier circuit shown in Fig. 5, and control voltage input node Vg thereof is supplied

with control voltage VG, which determines the level of the gate voltage of E-MES transistor J11 provided for amplification. Power amplifier circuit PAi may be any one of three power amplifier circuits PAa - PAc of power amplifier PA.

Gate voltage control circuit GVC has the same structure as that shown in Fig. 5. In Fig. 12A, gate voltage control circuit GVC includes voltage down circuit VD provided between an E-MES transistor E3 and positive power supply voltage Vdd. Voltage down circuit VD is provided for applying a voltage, which is lower than control voltage V1 applied to the gate of E-MES transistor E3, to the drain of E-MES transistor E3. This is because the reverse bias state between the gate and drain must be kept for operation of the MESFET. Reference voltage V1 for control is produced as disclosed in the foregoing prior art reference. More specifically, a constant current is generated by a current mirror circuit, and reference voltage V1 is generated by adjusting a current through the resistance element with this constant current. This constant current generating portion includes a diode for shifting the voltage level of control reference voltage V1 to a negative voltage level. Control voltage VG generates from output node OUT is a negative voltage. For example, negative voltage VSS is about −1.8 V, and control voltage VG is about −1.3 V.

Low pass filter 13 includes a transmission line TRL arranged in signal line G1 between output node OUT and input node VG, and capacitance element Cb arranged between signal line G1 and the ground node. Owing to provision of low pass filter 13 in signal transmission line G1 of control voltage VG, the radio-frequency leakage component can be reliably absorbed. More specifically, even if capacitance element C11 may not absorb the radio-frequency signal applied through capacitance element Cc or the radio-frequency component leaking through the gate of E-MES transistor J11 during the power amplification operation, low pass filter 13 can reliably absorb such radio-frequency leakage component. Therefore, control voltage VG can be held constant. Accordingly, it is possible to prevent generation of a reflected wave due to the radio-frequency leakage component on the output node OUT, and therefore variations in control voltage VG can be prevented so

that instable operation of circuit GVC can be prevented, and the bias point of E-MES transistor J11 can be stably held at the constant level.

Fig. 12B shows a structure of transmission line TRL shown in Fig. 12A. In Fig. 12B, transmission line TRL has a portion Pb having a smaller line width than portions Pa and Pc on the opposite sides thereof. For example, if line portions Pa and Pc of transmission line TRL have a line width d1 of 100 μm, line portion Pb has a line width d2 of, e.g., 20 μm. In transmission line TRL having the narrow portion, the narrow portion Pb suppresses passing of the radio-frequency component, and therefore equivalently provides an inductance L as shown in Fig. 12B.

Fig. 12C shows a structure of capacitance element Cb. Capacitance element Cb is formed of a metal interconnection layer Cb1 of a low resistance formed on a GaAs substrate 20, an insulating layer Cb2 formed on metal interconnection layer Cb1 and a metal interconnection layer Cb3 formed on insulating layer Cb2. Capacitance element Cb is a parallel-electrode MIM capacitor.

As shown in Fig. 12B, the inductance component is implemented by utilizing transmission line TRL. Therefore, the low pass filter can be implemented in a small occupying area without adding an element such as a coil. Assuming that transmission line TRL has an inductance of L, cut-off frequency of low pass filter 13 is given by the following formula:

$$fc = 1/2 \cdot \pi \cdot (L \cdot C)^{1/2}$$

A relationship of ($fc < fg/5$) may be satisfied.

In the structure shown in Fig. 12A, power amplifier circuit PAi and gate voltage control circuit GVC for controlling the gain of this amplifier are integrated on the same substrate. In this structure, the low pass filter is arranged in the signal line for transmitting the gate voltage, whereby the radio-frequency leakage component can be reliably restrained without increasing the occupied area so that the gate voltage control circuit can operate stably, and constant gate voltage VC can be produced stably.

[Modification]

Fig. 13 shows a structure according to a modification of the embodiment 2 of the invention. In the structure shown in Fig. 13, a resistance element Rg

is arranged in signal line G1 between control voltage output node OUT of gate voltage control circuit GVC and gate voltage input node Vg of power amplifier circuit PAi. In the structure shown in Fig. 13, therefore, a low pass filter 14 is formed of resistance element Rg and capacitance element Cb. Resistance element Rg is formed of an impurity diffusion region 21c located between heavily doped impurity regions 21a and 21b formed on GaAs substrate 20, as depicted by broken line in Fig. 13. Nodes 21d and 21e connected to heavily doped impurity regions 21a and 21b provide one and the other ends of resistance element Rg, respectively.

By using the diffusion resistance as resistance element Rg, the required resistance value can be achieved in a small occupied area. This is because GaAs substrate 20 is a semi-insulating substrate, and has an extremely high resistance value so that the required resistance value can be achieved easily in a small occupied area.

In the structure shown in Fig. 13, cut-off frequency fc is given by $1/(2 \cdot \pi \cdot Rg \cdot Cb)$ similarly to the foregoing embodiment 1. The relationship of ($fc < fg/5$) may be satisfied.

According to the structure in which low pass filter 14 is formed of resistance element Rg and capacitance element Cb as described above, the radio-frequency leakage component leaking from power amplifier circuit PAi can be easily absorbed with a small occupied area, and the gate voltage control circuit GVC can stably operate. Resistance element Rj may be added to output node OUT.

The low pass filter or the additional circuit of the embodiment 1 may be employed as the low pass filter of the embodiment 2, and the converse also holds.

According to the radio-frequency integrated circuit of the invention, as described above, the radio-frequency processing circuit and the control circuit controlling the operation of the radio-frequency processing circuit are integrated on the same chip, and particularly the low pass filter absorbing the radio-frequency component is arranged between the radio-frequency processing circuit and the control circuit. Therefore, the radio-frequency processing circuit can operate stably without an influence of the radio-

frequency leakage component.

Particularly in the transceiver such as a compact portable telephone, the low pass filter absorbing the radio-frequency component is arranged between the transmission/reception multiplexing switch and the control circuit controlling the operation modes of the transmission/reception multiplexing switch, whereby it is possible to suppress lowering of the handling power characteristics of the transmission/reception multiplexing switch as well as increase in power consumption of the control circuit.

Further, in the structure wherein the power amplifier performing the power amplification of the transmission signal and the negative voltage generating circuit controlling the gain of this power amplifier are arranged on the same chip, the gate voltage control circuit, which is included in the negative voltage generating circuit for controlling the gate voltage of the MESFET for amplification, can operate stably without an influence of the radio-frequency leakage component.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A radio-frequency integrated circuit, wherein a radio-frequency processing circuit (2: PAi) including a field effect transistor (J1 - J4; J11) receiving a radio-frequency input signal and transferring a signal corresponding to the radio-frequency input signal and a control voltage generating circuit (1; GVC) applying an operation control voltage (VR, VT; VG) to a gate of said field effect transistor through a path other than a transmission path of said radio-frequency input signal are integrated on a common substrate (RFFP), characterized in that a low pass filter (3; 8: 13; 14) for removing at least a signal in a frequency band of said radio-frequency input signal is arranged in said control voltage transmission path (SL1, SL2; SL21: G1).

2. The radio-frequency integrated circuit according to claim 1, wherein

said radio-frequency processing circuit is a transmission/reception multiplexing switch (2) having a transmission mode for transferring a radio-frequency signal (TX) applied to a transmission signal input node (Wt) to a transmission/reception node (Wa) coupled to an antenna (ANT) via a first field effect transistor (J2), and a reception mode for transferring a radio-frequency signal applied to said transmission/reception node to a reception signal output node (Wr) via a second field effect transistor (J3); and

said control voltage generating circuit (1: GVC) is a transmission/reception control circuit (1) for applying a control voltage for turning on and off the first and second field effect transistors in accordance with an operation mode.

3. The radio-frequency integrated circuit according to claim 1, wherein

said radio-frequency circuit (2: PAi) is a power amplifier (PAi) amplifying said radio-frequency input signal by said field effect transistor (J1), and

said control voltage generating circuit is a gate voltage control circuit (GVC) applying a bias voltage to a gate of said field effect transistor for

determining a gain of said power amplifier.

4. The radio-frequency integrated circuit according to claim 1, wherein said radio-frequency integrated circuit is an RF front end integrated circuit for processing a signal in a frequency band of a carrier wave of transmission and reception signals in a portable telephone.

5. An radio-frequency integrated circuit, including

(i) a transmission/reception multiplexing switch circuit (2) having a transmission signal input node (Wt), a reception signal output node (Wr) and a control signal input node (Wc) provided separately from said transmission signal input node and said reception signal output node, and operating in accordance with a control signal applied to said control signal input node in either a transmission mode for transmitting a transmission signal applied to said transmission signal input node and a reception mode for receiving and sending a coming signal to said reception signal output node, and (ii) a control circuit (1) generating said control signal to the control signal input node of said transmission/reception multiplexing switch circuit (2) in response to an operation mode instructing signal (ϕT, ϕR) are integrated on a common chip (RFFP), characterized in that

low pass filter (3; 3a, 3b; 8) allowing passing of a signal in a band lower than a frequency band of the transmission signal applied to said transmission signal input node is arranged between said control circuit and said control signal input node of said transmission/reception multiplexing switch.

6. The radio-frequency integrated circuit according to claim 5, wherein said multiplexing switch circuit (2) includes a switch element (J1 - J4) receiving said control signal (VR, VT) on a control electrode node through a resistance element (Ra: R1 - R4), and coupling one of said transmission signal input node (Wt) and said reception signal output node (Wr) to a transmission/reception node (Wa) electrically coupled to an antenna,

said low pass filter (3; 3a, 3b; 8) includes a capacitance element (Ct, Cr; Ca) connected between a reference potential source (gnd) and an

interconnection line (SLa, SL2) between a control signal output node (Vout1, Vout2) of said control circuit and said resistance element (R1 - R4), and said resistance element (R1 - R4) functions as a component of said low pass filter.

7. The radio-frequency integrated circuit according to claim 6, wherein said switch element (J1 - J4) includes;

a first switch element (J2, J4) for transmitting a transmission signal (TX) applied to said transmission signal input node to said transmission/reception node (Wa), and

a second switch element (J1, J3) for transmitting a signal applied to said transmission/reception node to said reception signal output node (Wr):

said control circuit (1) includes;

circuitry (1a, 1b) for generating first and second control signals (VT, VR) for activating and deactivating the first and second switch elements in accordance with said operation mode instructing signal (ϕT, ϕR): and

said low pass filter is arranged in each of paths (SL1, SL2) transmitting said first and second control signals.

8. The radio-frequency integrated circuit according to claim 6, wherein said switch element (J1 - J4) includes;

a first switch element (J2, J4) for transmitting a transmission signal applied to said transmission signal input node (Wt) to said transmission/reception node (Wa), and

a second switch element (J1, J3) for transmitting a coming signal applied to said transmission/reception node to said reception signal output node (Wr):

said control circuit (1) includes;

means (1a, 1b) for generating first and second control signals (VT, VR) for turning on and off the first and second switch elements in accordance with said operation mode instructing signal (ϕT, ϕR): and

said low pass filter (3a, 3b; 8) is arranged in a path (SL2) transmitting said second control signal (VR).

9. The radio-frequency integrated circuit according to claim 6, wherein

said control circuit (1) includes means (1a, 1b) for generating a first control signal (VT) being active in a transmission mode and a second control signal (VR) being active in a reception mode:

said switch element (J1 - J4) includes;

a first switching transistor (J2) being turned on to couple said transmission signal input node (Wt) to said transmission/reception node (Wa) when said first control signal is active,

a second switching transistor (J1) being turned on to couple said transmission signal input node to a reference potential source (gnd) when said second control signal is active,

a third switching transistor (J3) being turned on to transmit the signal on said transmission/reception node to said reception signal output node (Wr) when said second control signal is active, and

a fourth switching transistor (J4) being turned on to transfer the signal on said reception signal output node to said reference potential source when said first control signal is active: and

said low pass filter (3; 8) is arranged only in a transmission path (SL) transmitting said second control signal (VR) to a control electrode node of said second switching transistor (J1).

10. The radio-frequency integrated circuit according to any one of claims 6 to 9, wherein

a capacitance value Ca of said capacitor (Cr, Ct; Ca) and a resistance value Ra of said resistance element (R1 - R4) satisfy a relationship of:

$1/(2 \cdot \pi \cdot Ca) < (fg \cdot Ra/5)$,

where fg represents a frequency of the transmission signal (TX) applied to said transmission signal input node (Wt).

11. The radio-frequency integrated circuit according to any one of claims 6 to 9, wherein

a capacitance value Ca of said capacitor element (Cr, Ct; Ca) and a resistance value Ra of said resistance element (R1 - R4) satisfy a relationship

of:

$$fg \cdot Ra/100 < 1/(2 \cdot \pi \cdot Ca) < (fg \cdot Ra/5)$$

where fg represents a frequency of the transmission signal (TX) applied to said transmission signal input node (Wt).

12. The radio-frequency integrated circuit according to any one of claims 6 to 11, wherein

said low pass filter means (3; 3a, 3b; 8) further includes an additional resistance element (R, R7; Rb) arranged on said interconnection line and between the control signal output node (Vout1, Vout2) of said control circuit (1) (VT, VR) and a connection node between said capacitance element (Cr, Ct; Ca) and said interconnection line.

13. The radio-frequency integrated circuit according to claim 12, wherein

a resistance value Ra of said resistance element (R1 - R4) and a resistance value Rb of said additional resistance element (R6, R7; Rb) satisfy a relationship of:

$$Rb < Ra/5$$

14. The radio-frequency integrated circuit according to claim 5, further comprising:

an amplifier (PAi) for amplifying and transmitting a radio-frequency signal to said transmission signal input node (Wt);

bias voltage generator (VGC) for generating a bias voltage controlling a gain of said amplifier; and

a second low pass filter (13; 14) arranged between a bias voltage output node (out) of said bias voltage generator and a bias voltage input node (Vg) of said amplifier.

15. The radio-frequency integrated circuit according to claim 14, wherein

said second low pass filter (13; 14) includes:

a transmission line (TRL) connected between said bias voltage output node (out) and said bias voltage input node (Vg) for transmitting said bias voltage (VG), and having a portion smaller in width than other portion; and

a capacitance element (Cb) connected between said bias voltage output node and a reference potential source.

16. The radio-frequency integrated circuit according to claim 14, wherein

said second low pass filter (13; 14) includes:

a resistance element (Rg) connected between said bias voltage output node (out) and said bias voltage input node (Vg); and

a capacitance element (Cb) connected between said bias voltage output node and a reference potential source (gnd).

17. A radio-frequency integrated circuit, including an amplifier (PAi) amplifying a power of a radio-frequency signal and a bias voltage generating circuit (VGC) generating a bias voltage (VG) for controlling a gain of said amplifier to a bias voltage input node (Vg) of said amplifier integrated on a common substrate, comprising:

a low pass filter (13; 14) connected between a bias voltage input node (Vg) of said amplifier and a bias voltage output node (out) of said bias voltage generating circuit.

18. The radio-frequency integrated circuit according to claim 17, wherein

said amplifier (PAi) includes a field effect transistor (J11) amplifying said radio-frequency signal received on a control gate node thereof, and the bias voltage (VG) generated by said bias voltage generating circuit (VGC) is a negative voltage applied to the gate of said field effect transistor.

19. The radio-frequency integrated circuit according to claim 17, wherein

said low pass filter includes a transmission line (TRL) connected

between an output node (out) of said bias voltage generating circuit (VGC) and the bias voltage input node (Vg) of said amplifier (PAi) for transmitting said bias voltage, and having a portion smaller in width than other portion; and a capacitance element (Cb) connected between said bias voltage output node (out) and a reference potential source (gnd).

20. The radio-frequency integrated circuit according to claim 17, wherein

said low pass filter (13; 14) includes:

a resistance element (Rg) connected between the bias voltage output node (out) of said bias voltage generating circuit (VGC) and the bias voltage input node (Vg) of said amplifier (PAi); and

a capacitance element (Cb) connected between said bias voltage output node (out) and a reference potential source (gnd).

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP96/02208

A. CLASSIFICATION OF SUBJECT MATTER
Int. Cl^6 H03G3/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int. Cl^6 H03G3/20, H04B1/44, H01P1/15, H03F3/19, H03K17/687, H03H7/01

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926 - 1996
Kokai Jitsuyo Shinan Koho 1971 - 1996

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 7-74604, A (Murata MFG. Co., Ltd.), March 17, 1995 (17. 03. 95), Page 2, left column, line 34 to right column, line 33; Fig. 5 (Family: none)	1, 2, 4-13
Y	JP, 5-43622, U (Toshiba Corp.), June 11, 1993 (11. 06. 93), Figs. 1, 2 (Family: none)	1, 2, 4-13
Y	JP, 8-70245, A (Hitachi, Ltd.), March 12, 1996 (12. 03. 96), Page 2, right column, lines 23 to 34 & EP, 700161, A2	4, 6, 9, 10-13
Y	JP, 5-199094, A (Sharp Corp.), August 6, 1993 (06. 08. 93), Page 3, left column, line 26 to right column, line 41 (Family: none)	4, 6, 9, 10-13
Y	JP, 62-147931, U (Mitsubishi Electric Corp.), September 18, 1987 (18. 09. 87),	1, 2, 4-13

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
October 29, 1996 (29. 10. 96)	November 19, 1996 (19. 11. 96)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Figs. 1, 3 (Family: none)	
Y	JP, 7-202585, A (NEC Corp.), August 4, 1995 (04. 08. 95), Page 3, left column, lines 24 to 27 (Family: none)	1, 3, 14, 15, 17-19
Y	JP, 55-91216, A (Fujitsu Ltd.), July 10, 1980 (10. 07. 80), Page 1, right column, lines 3 to 16; page 2, right column, lines 1 to 16 (Family: none)	1, 3, 14-17, 19, 20
Y	JP, 3-192801, A (Mitsubishi Electric Corp.), August 22, 1991 (22. 08. 91), Page 1, right column, lines 12 to 19 (Family: none)	1, 3, 14-17, 20
Y	JP, 3-261205, A (Kokusai Electric Co., Ltd.), November 21, 1991 (21. 11. 91), Figs. 1, 2 (Family: none)	1, 3, 14, 17
Y	JP, 51-134084, A (Takanobu Matsumoto, Director General, Agency of Industrial Science and Technology), November 20, 1976 (20. 11. 76), Page 1, right column, lines 13 to 15 (Family: none)	15, 19